EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	57	taketo near heishi.in.	US-PGPUB; USPAT	OR	ON	2007/08/14 14:07
S2	58	hajime near ogawa.in.	US-PGPUB; USPAT	OR	ON	2007/08/14 14:08
S3	9	takenobu near tani.in.	US-PGPUB; USPAT	OR	ON	2007/08/14 14:09
S4	12	yukihiro near sasagawa.in.	US-PGPUB; USPAT	OR	ON	2007/08/14 14:10
S5	36966	matsushita.as.	US-PGPUB; USPAT	OR	ON	2007/08/14 14:10
S6	5	S5 and (pars$4 and optimiz$5).clm.	US-PGPUB; USPAT	OR	ON	2007/08/14 14:12
S7	10	S5 and (compiler and optimiz$5).clm.	US-PGPUB; USPAT	OR	ON	2007/08/14 14:15
S8	2	("20020161986"|"5790874").PN.	US-PGPUB; USPAT	OR	ON	2007/08/14 14:15
S9	14	("3478322" | "3792441" | "4204252" | "5274829").PN. OR ("5790874").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/08/14 14:39
S10	50	("5442760" "5202975" "5488729" "5640588" "5884060" "5966537" "5185868" "5251306" "5307478" "5404469" "5471593" "5481743" "5630083" "5655096" "5717883" "5812810" "5826096" "5852741" "5862399" "5923871" "5974537" "6002880" "6009483" "6044451" "6076154" "6122722" "6658551" "6665791" "6886091" "7058937" "7082602" "7096343" "7134028" "20020083313" "20020161987" "20030196197" "20030200539" "20040154006" "20040221185" "20050251648" "5369774" "5404552" "5577256" "5642512" "5790862" "5815698" "6035122" "6085306" "6131145" "6141791").pn.	US-PGPUB; USPAT; USOCR	OR	ON	2007/08/14 14:39
S11	3839	717/140-161.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/14 14:54

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S12	7	S11 and (ham$4 near distance)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/14 15:01
S13	35	(ham$4 near distance) and compiler and dependency	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/14 15:13
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S15	23	S14 and compiler	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/14 15:13
S16	76	(stop$4 near instruction) and (resume near instruction)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/15 13:33
S17	20	S16 and compiler	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/15 13:31

Terms used: **hamming distance compiler** Found **6,540** of **207,474**

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1 Memories: A post-compilation register reassignment technique for improving hamming distance code compression

Montserrat Ros, Peter Sutton

September 2005 **Proceedings of the 2005 international conference on Compilers, architectures and synthesis for embedded systems CASES '05**

Publisher: ACM Press

Full text available: pdf(193.16 KB) Additional Information: full citation, abstract, references, index terms

Code compression is a field where compression ratios between compiler-generated code and subsequent compressed code are highly dependent on decisions made at compile time. Most optimizations employed by compilers tend to focus on parameters such as program performance, minimizing resource dependencies and sometimes the option of reducing code size.This paper describes a post-compilation technique for the greedy reassignment of general purpose scratch registers to improve Hamming distance based c ...

Keywords: code compression, hamming distance, register reassignment

2 Low power processors: A hamming distance based VLIW/EPIC code compression technique

Montserrat Ros, Peter Sutton

September 2004 **Proceedings of the 2004 international conference on Compilers, architecture, and synthesis for embedded systems CASES '04**

Publisher: ACM Press

Full text available: pdf(132.73 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents and reports on a VLIW code compression technique based on vector Hamming distances. It investigates the appropriate selection of dictionary vectors such that all program vectors are at most a specified maximum Hamming distance from a dictionary vector. Bit toggling information is used to restore the original vector.A dictionary vector selection method which considered both vector frequency as well as maximum coverage achieved better results than just considering vector freque ...

Keywords: VLIW, code compression, hamming distance

3 Compiler optimization on VLIW instruction scheduling for low power

Chingren Lee, Jenq Kuen Lee, Tingting Hwang, Shi-Chun Tsai

April 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 2

Publisher: ACM Press

Full text available: pdf(175.72 KB) Additional Information: full citation, abstract, references, citings, index terms, review

In this article, we investigate compiler transformation techniques regarding the problem of scheduling VLIW instructions aimed at reducing power consumption of VLIW architectures in the instruction bus. The problem can be categorized into two types: horizontal scheduling and vertical scheduling. For the case of horizontal scheduling, we propose a bipartite-matching scheme for instruction scheduling. We prove that our greedy bipartite-matching scheme always gives the optimal switching activities ...

Keywords: Compilers, VLIW instruction scheduling, instruction bus optimizations, low-power optimization

4 Code generation and scheduling: Compiler optimization on instruction scheduling for low power

Chingren Lee, Jenq Kuen Lee, TingTing Hwang, Shi-Chun Tsai

September 2000 **Proceedings of the 13th international symposium on System synthesis ISSS '00**

Publisher: IEEE Computer Society

Full text available: pdf(375.33 KB) Additional Information: full citation, abstract, references, citings

In this paper, we investigate the compiler transformation techniques to the problem of scheduling VLIW instructions aimed to reduce the power consumption on the instruction bus. It can be categorized into two types: horizontal and vertical scheduling. For the horizontal case, we propose a bipartite-matching scheme. We prove that our greedy algorithm always gives the optimal switching activities of the instruction bus. In the vertical case, we prove that the problem is NP-hard, and propose a heur ...

5 Instruction execution sequence confirmation

Kay P. Litchfield

June 1994 **ACM SIGARCH Computer Architecture News**, Volume 22 Issue 3

Publisher: ACM Press

Full text available: pdf(382.00 KB) Additional Information: full citation, abstract, index terms

Acquiring extremely dependable results from computers requires attention to all of the stages from program and machine design through execution of the program. One of the smaller, but still important, stages is that of verifying that the sequence of instructions executed by the processor was exactly the sequence specified by the compiler. A surprisingly small addition to the logic of the processor (and code produced by the compiler) is sufficient to achieve this.

6 Power and performance optimizations on system level design: A bitmask-based code compression technique for embedded systems

Seok-Won Seong, Prabhat Mishra

November 2006 **Proceedings of the 2006 IEEE/ACM international conference on Computer-aided design ICCAD '06**

Publisher: ACM Press

Full text available: pdf(153.50 KB) Additional Information: full citation, abstract, references, index terms

Embedded systems are constrained by the available memory. Code compression techniques address this issue by reducing the code size of application programs. Dictionary-based code compression techniques are popular because they offer both good compression ratio and fast decompression scheme. Recently proposed techniques [8, 9] improve standard dictionary-based compression by consideringmismatches. This paper makes two important contributions: i) it provides a cost-benefit analysis framework for ...

7 On finding the closest bitwise matches in a fixed set

Peter Klier, Richard J. Fateman

March 1991 **ACM Transactions on Mathematical Software (TOMS)**, Volume 17 Issue 1

Publisher: ACM Press

Full text available: pdf(676.14 KB) Additional Information: full citation, abstract, references, index terms, review

In a given large fixed table of bit-vectors, we would like to find, as rapidly as possible, those bit-vectors which have the least Hamming distances from a newly-presented arbitrary bit-vector.

Keywords: Hamming distance, K-d trees, bit-vectors, hash-table, high-dimension search, pattern matching, search

8 The design and use of simplepower: a cycle-accurate energy estimation tool

W. Ye, N. Vijaykrishnan, M. Kandemir, M. J. Irwin

June 2000 **Proceedings of the 37th conference on Design automation DAC '00**

Publisher: ACM Press

Full text available: pdf(207.45 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we presen t the design and use of a comprehensiv e framework, SimplePower, for ev aluating the effect of high-level algorithmic, architectural, and compilation trade-offs on energy. An execution-driven, cycle-accurate RT lev el energy estimation tool that uses transition sensitive energy models forms the cornerstone of this framework. SimplePower also pro vides the energy consumed in the memory system and on-chip buses using analytical energy ...

9 Genetic algorithms: papers: Geometric crossover for multiway graph partitioning

Yong-Hyuk Kim, Yourim Yoon, Alberto Moraglio, Byung-Ro Moon

July 2006 **Proceedings of the 8th annual conference on Genetic and evolutionary computation GECCO '06**

Publisher: ACM Press

Full text available: pdf(258.95 KB) Additional Information: full citation, abstract, references, index terms

Geometric crossover is a representation-independent generalization of the traditional crossover defined using the distance of the solution space. Using a distance tailored to the problem at hand, the formal definition of geometric crossover allows to design new problem-specific crossovers that embed problem-knowledge in the search. The standard encoding for multiway graph partitioning is highly redundant: each solution has a number of representations, one for each way of labeling the represented ...

Keywords: geometric crossover, labeling-independent distance, multiway graph partitioning

10 A bibliography on syntax error handling in context free languages

Peter N. van den Bosch

April 1992 **ACM SIGPLAN Notices**, Volume 27 Issue 4

Publisher: ACM Press

Full text available: pdf(918.30 KB) Additional Information: full citation, index terms

11 Address bus encoding techniques for system-level power optimization

L. Benini, G. De Micheli, E. Macii, D. Sciuto, C. Silvano

February 1998 **Proceedings of the conference on Design, automation and test in Europe DATE '98**

Publisher: IEEE Computer Society

Full text available: pdf(196.30 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

The power dissipated by system-level buses is the largest contribution to the global power of complex VLSI circuits. Therefore, the minimization of the switching activity at the I/O interfaces can provide significant savings on the overall power budget. This paper presents innovative encoding techniques suitable for minimizing the switching activity of system-level address buses. In particular, the schemes illustrated here target the reduction of the average number of bus line transitions per cl ...

12 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Publisher: ACM Press

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

13 Dynamic Functional Unit Assignment for Low Power

Steve Haga, Natasha Reeves, Rajeev Barua, Diana Marculescu

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**

Publisher: IEEE Computer Society

Full text available: pdf(175.35 KB) Publisher Site Additional Information: full citation, abstract, citings, index terms

A hardware method for functional unit assignment is presented, based on the principle that a functional unitýs power consumption is approximated by the switching activity of its inputs. Since computing the Hamming distance of the inputs in hardware is expensive, only a portion of the inputs are examined. Integers often have many identical top bits, due to sign extension, and floating points often have many zeros in the least significant digits, due to the casting of integer values into floating ...

14 Interactive presentation: Activity clustering for leakage management in SPMs

M. Kandemir, G. Chen, F. Li, M. J. Irwin, I. Kolcu

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(111.19 KB) Additional Information: full citation, abstract, references

This paper we proposes compiler-based leakage optimization strategy for on-chip scratch-pad memories (SPMs). The idea is to keep only a small set of SPM regions active at a given time and pre-activate SPM regions based on the compiler-extracted data access pattern. Our strategy, called activity clustering, increases the length of the idle periods of SPM regions by clustering accesses to a small set of regions at a time. It thus allows an SPM to take better advantage of the underlying leakage opt ...

15 Compiler-Based Register Name Adjustment for Low-Power Embedded Processors

Peter Petrov, Alex Orailoglu

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design ICCAD '03**

Publisher: IEEE Computer Society

Full text available: pdf(202.54 KB) Additional Information: full citation, abstract, citings, index terms

We present an algorithm for compiler-driven register name adjustmentwith the main goal of power minimization on instruction fetchand register file access. In most instruction set architecture (ISA) designs,the register fields reside in fixed positions within the

instructionencoding, hence forming streams of indices on the instruction bus andto the register file address decoder. The number of bit transitions inthese streams greatly determines the power consumption on the addressbus and the regist ...

16 Power optimization and management in embedded systems

Massoud Pedram

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation ASP-DAC '01**

Publisher: ACM Press

Full text available: pdf(91.36 KB) Additional Information: full citation, abstract, references, citings, index terms

Power-efficient design requires reducing power dissipation in all parts of the design and during all stages of the design process subject to constraints on the system performance and quality of service (QoS). Power-aware high-level language compilers, dynamic power management policies, memory management schemes, bus encoding techniques, and hardware design tools are needed to meet these often-conflicting design requirements. This paper reviews techniques and tools for power-efficient embedd ...

17 Finding effective compilation sequences

L. Almagor, Keith D. Cooper, Alexander Grosul, Timothy J. Harvey, Steven W. Reeves, Devika Subramanian, Linda Torczon, Todd Waterman

June 2004 **ACM SIGPLAN Notices , Proceedings of the 2004 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems LCTES '04**, Volume 39 Issue 7

Publisher: ACM Press

Full text available: pdf(743.88 KB) Additional Information: full citation, abstract, references, citings, index terms

Most modern compilers operate by applying a fixed, program-independent sequence of optimizations to all programs. Compiler writers choose a single "compilation sequence", or perhaps a couple of compilation sequences. In choosing a sequence, they may consider performance of benchmarks or other important codes. These sequences are intended as general-purpose tools, accessible through command-line flags such as -O2 and -O3.Specific compilation sequences make a significant difference in the quality ...

Keywords: adaptive compilers, learning models

18 Algorithms for the optimal loading of recursive neural nets

V. Chandru, A. Dattasharma, S. S. Keerthi, N. K. Sancheti, V. Vinay

January 1995 **Proceedings of the sixth annual ACM-SIAM symposium on Discrete algorithms SODA '95**

Publisher: Society for Industrial and Applied Mathematics

Full text available: pdf(918.30 KB) Additional Information: full citation, references, index terms

19 DB-4 (databases): similarity search: Localized signature table: fast similarity search on transaction data

Qiang Jing, Rui Yang, Panos Kalnis, Anthony K. H. Tung

November 2004 **Proceedings of the thirteenth ACM international conference on Information and knowledge management CIKM '04**

Publisher: ACM Press

Full text available: pdf(200.77 KB) Additional Information: full citation, abstract, references, index terms

Recently, techniques for supporting efficient similarity search over huge transaction datasets have emerged as an important research area. Several indexing schemes have been proposed towards this direction. Typically, these schemes provide a tradeoff between searching efficiency and indexing overhead in terms of space.

In this paper, we propose a novel indexing scheme for similarity search on transaction data. Based on well-studied clustering techniques, we develop a construction algor ...

Keywords: data mining, indexing, similarity search, transaction data

20 High-cost CFD on a low-cost cluster

Thomas Hauser, Timothy I. Mattox, Raymond P. LeBeau, Henry G. Dietz, P. George Huang
November 2000 **Proceedings of the 2000 ACM/IEEE conference on Supercomputing (CDROM) Supercomputing '00**
Publisher: IEEE Computer Society
Full text available: pdf(4.00 MB) Additional Information: full citation, abstract, references, index terms
Publisher Site

Direct numerical simulation of the Navier-Stokes equations (DNS) is an important technique for the future of computational fluid dynamics (CFD) in engineering applications. However, DNS requires massive computing resources. This paper presents a new approach for implementing high-cost DNS CFD using low-cost cluster hardware. After describing the DNS CFD code DNSTool, the paper focuses on the techniques and tools that we have developed to customize the performance of a cluster ...

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